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EXAMINER

WARREN, MATTHEW E

ART UNIT PAPER NUMBER

2815

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/733,781

Applicant(s)

PATTI

Examiner

Matthew E. Warren

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 20 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-7 and 20-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-7, 20-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

This Office Action is in response to the Amendment filed on May 20, 2203.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 4-7, 20-23 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP 06-342878 A) in view of Sakai et al. (JP 61-232657 A).

Ito discloses (abstract and fig. 1) an integrated circuit device comprising a high voltage resistor (R) integrated in a semiconductor material body (12) in which the resistor has a vertical current flow. The resistor has the same conductivity type (N) as the semiconductor material body and is formed by a portion of the semiconductor material body extending between a first (top) surface (14) and second (bottom) surface (10) of the body. Ito shows all of the elements of the claims except the resistor delimited at least partially by an insulation region extending from the first surface towards a second surface. Sakai et al. discloses (abstract and figs. 1 and 2 on page 3) an integrated circuit device comprising a high voltage resistor (R) integrated in a semiconductor material body (3). The resistor has the same conductivity type (N) as the semiconductor material body and is formed by a portion of the semiconductor material body extending between a first (top) surface and second (bottom) surface of the body.

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The resistor is delimited at least partially by an insulation region (11) extending from the first surface towards the second surface of the body. The insulating region has a closed shape and is formed of isolating material. A first and second region (regions 5 on each side of insulator 11) having a conductivity type opposite (P) that of the material body is arranged on opposite sides of the insulation region. First and second electronic devices (Q1 and Q2 [not shown in fig. 1]) are formed on opposite sides of the insulation region. The insulating region is open at a bottom portion such that the semiconductor region (3) is contiguous with the semiconductor body (1). The semiconductor region has a rectangular cross section and the insulating region has a rectangular frame shape. The semiconductor region (3) includes an upper region (6) adjacent to the surface of the semiconductor body and a lower region (3) below the upper region, wherein the upper region is doped at a higher doping level (n+) than the lower region (n). The semiconductor region also includes an upper region (5) adjacent to the surface of the semiconductor body and a lower region (2) positioned below the upper region, wherein the upper region has a conductivity type (p) opposite to the conductivity type (n) of the lower region, inherently forming a diode. This configuration helps increase the electrostatic breakdown capacity. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the vertical resistor Ito by forming the resistor between two isolation regions as taught by Sakai to increase the electrostatic breakdown capacity of an ESD device.

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Claims 24, 25, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (JP 06-342878 A) in view of Sakai et al. (JP 61-232657 A) as applied to claims 1 and 20 above, and further in view of Sivan (US 5,229,310).

Ito in view of Sakai et al. shows all of the elements of the claims except the insulating region having conductive filler surrounded by insulating walls. Sivan shows (fig. 1F) a semiconductor device having a trench lined with insulating material (32) and conductive filler (38) surrounded by the insulating walls. The region also includes an upper region (28) of a first conductivity type, a middle region of a second conductivity type, and lower region (26) also of the first conductivity type. The upper and lower regions operate as source/drain regions and the conductive material (38) functions as a gate electrode (col. 5, lines 12-21 and col. 6, lines 11-30). This configuration minimizes the transistor size and ultimately increases the cell density. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the insulation region of Ito and Sakai by filling the layer with conductive material as a gate as taught by Sivan to reduce the transistor size and increase the cell density.

### ***Response to Arguments***

Applicant's arguments filed with respect to claims 1, 2, 4-7, and 20-30 have been fully considered but they are not persuasive. The applicant primarily argues that the references do not show all of the elements of the claims, specifically that Sakai teaches a horizontal resistor and cannot be combined with Ito and that Sivan does not disclose the limitations of claim 25. The examiner believes that the cited references show all of

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the elements of the claims. Sakai can be combined with Ito because a vertical resistor is taught. This is evident in the abstract of Sakai when it is stated "An N-type region in a P-N junction forming a resistor R is not connected to an N+ type collector contact layer 2, but connected to a P-type substrate 1 by surrounding the periphery of the insulating layer 10 as an element isolation region, thus forming a vertical type P-N-P parasitic transistor." This means that the resistor, which would normally be connected laterally to N+ region 2 in figure 2 of Sakai, is connected vertically and is part of the vertical P-N-P transistor. The addition of the isolation layer forms the resistor/parasitic transistor vertically. Even if one of ordinary skill in the art were not to use the teaching of the resistor of Sakai, one would use the isolation layer of Sakai to laterally separate the resistor from the N-type contact layer. Thus, the isolation regions of Sakai are applicable to Ito to at least isolate desired components but also improve the electrostatic resistance.

In re the arguments pertaining to claims 29 and 30, the rejection of those claims was mistakenly added to the rejection of claim 1. However, the limitations of claims 29 and 30 are the same as the limitations of claims 24 and 25, which were properly rejected further in view of Sivan. Thus the arguments of claims 24 and 25 also pertain to claims 29 and 30. The examiner believes that Sivan discloses all the limitations of claims 24, 25, 29, and 30. For instance claim 25 states that the "semiconductor region (which is laterally surrounded by the insulating region) includes an upper region of a first conductivity type; a middle region of a second conductivity type...and a lower region of the first conductivity type...such that a transistor is formed that includes the conductive

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filler as a gate, the upper region as a first source/drain region, and the lower region as a second source/drain region.” It is understood by the examiner that the upper, middle, and lower regions of Sivan are not formed in the same manner as those regions of the applicant’s invention, however, the claims don’t specifically recite a distinctive structure. The claims broadly state that the “semiconductor region includes...” Because Ito in view of Sakai already disclosed the insulating region surrounding the semiconductor region, it was not necessary for Sivan to disclose that limitation. Sivan was primarily cited to show the conductive filler in the insulating region and the upper, middle, and lower region in the semiconductor regions. Figure 1F of Sivan showed that the semiconductor region (thin film layer) included an upper region (28), middle region (30) and lower region (26). The upper and lower regions have the same conductivity type and are used as source/drain regions (col. 5, lines 15-21). The so-called first and second current electrodes are sources and drains. The single configuration of Sivan could be applied each insulator of Ito in view of Sakai and all limitations would be met since it is only necessary to show the missing limitation of the conductive filling and 3 regions. Additionally, another embodiment of Sivan is shown in figure 4 in which a semiconductor region is surrounded by two insulation regions, each having the conductive filler as a gate. Sivan cures the deficiencies of Ito and Sakai and shows motivation for forming the gate in the insulation layer. The combined references show all of the elements of the claims and this action is made final.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (703) 305-0760. The examiner can normally be reached on Mon-Thurs, and alternating Fri, 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 308-7722 for After Final communications.



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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

MEW

*MEW*

August 4, 2003



EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
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